UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/534,903	05/16/2005	Ramkrishnan Wenkata Subramanian	1890-0248	2393

50255 7590 08/08/2007

MAGINOT, MOOR & BECK
111 MONUMENT CIRCLE, SUITE 3000
BANK ONE CENTER/TOWER
INDIANAPOLIS, IN 46204

EXAMINER	
PARK, JEONG S	

ART UNIT	PAPER NUMBER
2154	

MAIL DATE	DELIVERY MODE
08/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/534,903	WENKATA SUBRAMANIAN ET AL.	
	Examiner	Art Unit	
	Jeong S. Park	2154	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *5/16/2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/26/2005, 12/16/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 9-28 are objected to because of the following informalities:

In claim 9, line 5, the word "the locations" should be corrected as –the plurality of locations-- for clear understanding of the claim. Similar correction should be made for claim 21, line 4;

In claim 9, line 8, the phrase "a stored data packet" should be corrected as –the first data packet of the first message-- for clear understanding of the claim;

In claim 9, line 9, the phrase "one other stored data packet" should be corrected as –the one other data packet of the first message-- for clear understanding of the claim;

In claim 16, line 14, the phrase "a stored data packet" should be corrected as –the one other data packet-- for clear understanding of the claim;

In claim 21, line 7, the word "data" should be corrected as –the first data packet of the first message-- for clear understanding of the claim;

In claim 21, line 8, the phrase "other data" should be corrected as –the one or more other data packets of the first message -- for clear understanding of the claim;

In claim 26, line 10, the word "data" should be corrected as –the first data packet of the message-- for clear understanding of the claim; and

In claim 26, line 11, the phrase "other data" should be corrected as –the one other data packet of the message-- for clear understanding of the claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 9, 11, 13, 14, 16, 18, 20, 21, 23, 25 and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by Bolan al. (hereinafter Bolan)(U.S. Patent No. 5,210,828).

Regarding claims 9, 21 and 25, Bolan teaches as follows:

A mailbox apparatus or a method (interprocessor communication facility 50 contains arbitration circuitry 60, mailbox circuitry 100 and processor interrupt circuitry 100 in figure 1, see, e.g., col. 3, lines 56-58) for temporally storing messages (mailbox circuitry receives message from sending processors and provides them to the intended receiving processors, see, e.g., col. 5, lines 6-9), each message including a sequence of one or more data packets being transferred between a plurality of locations (segmentation is inherent for large message size depending on the bus transferring capability), the mailbox apparatus (interprocessor communication facility, 50 in figure 1 and 2) including a main memory (holding register, 61-63 in figure 2), an ancillary memory (mailbox array 105 and message output register 160 in figure 2)(see, e.g., col. 5, lines 6-16 and figure 2), and a control unit which is arranged to:

Receive a first message from one of the locations (arbitration circuitry, 60 in figure 2, decodes the commands sent from the processors through communication bus

41-43 and routes them either to processor interrupt circuitry or to mailbox circuitry, see, e.g., col. 3, line 67 to col. 4, line 4);

Store at least a first data packet of the first message in the ancillary memory (mailbox array 105 and message output register 160 in figure 2) and at least one other data packet of the first message in the main memory (holding register, 61-63 in figure 2)(see, e.g., col. 6, lines 36-57); and

In response to a read signal (read message commend), transmit a stored data packet from the ancillary memory to another location (message output register sends the message to the processor who issued the read commend), and replenish the ancillary memory by transferring at least one other stored data packet to the ancillary memory from the main memory (message is retrieved from the addressed mailbox entry and placed in message output register)(see, e.g., col. 6, lines 48-57).

Regarding claims 11, 18 and 23, Bolan teaches as follows:

The ancillary memory (mailbox circuitry) is implemented as registers (message output register, see, e.g., col. 5, lines 10-12).

Regarding claims 13 and 20, Bolan teaches as follows:

The ancillary memory is configured to store a number of data packets which is at least equal to a number of clock periods required to extract any data packet from the main memory (four clock cycles to decode and execute a command, see, e.g., col. 5, lines 56-68, therefore each clock cycle completes one extraction of data packet from the main memory for write/read commands).

Regarding claim 14, Bolan teaches as follows:

A plurality of ancillary memories (mailbox portions, 110, 120 and 130 in figure 2), each ancillary memory having a distinct corresponding locations, each ancillary memory being arranged to store data packets to be transmitted to the corresponding location (mailbox array, 105 in figure 2, contains mailbox portions, which are reserved for the use of processors, 10, 20 and 30 in figure 2, see, e.g., col. 5, lines 12-18).

Regarding claims 16 and 26, Bolan teaches as follows:

A plurality of processors or a method (10, 20 and 30 in figures 1 and 2) and a mailbox apparatus (interprocessor communication facility 50 contains arbitration circuitry 60, mailbox circuitry 100 and processor interrupt circuitry 100 in figure 1, see, e.g., col. 3, lines 56-58), a first processor (processor 10 in figure 2) of the plurality of processors being arranged to transfer a message to a second processor (processor 20 in figure 2) of the plurality of processors by transmitting the message as a series of data packets to the mailbox apparatus (mailbox circuitry 100 in figure 2) and sending a signal (interrupt signal) to the second processor to indicate the presence of the message in the mailbox apparatus (sends an interrupt to processor 20 indicating a synchronous message is in the mailbox waiting for processing, see, e.g., col. 9, lines 14-20), the second processor being arranged in response to send a read signal to the mailbox apparatus (processor 20 use a read message command to get the message, see, e.g., col. 9, lines 20-21)(synchronous message transaction between processor 10 to processor 20, see, e.g., col. 8, line 63 to col. 9, line 33);

The mail box apparatus comprising a main memory, an ancillary memory, and a control unit which is arranged to (see, e.g., col. 5, lines 6-16 and figure 2);

Receive the message from the first processor (arbitration circuitry, 60 in figure 2, decodes the commands sent from the processors through communication bus 41-43 and routes them either to processor interrupt circuitry or to mailbox circuitry, see, e.g., col. 3, line 67 to col. 4, line 4);

Store at least a first data packet of the message in the ancillary memory (mailbox array 105 and message output register 160 in figure 2) and at least one other data packet of the message in the main memory (holding register, 61-63 in figure 2)(see, e.g., col. 6, lines 36-57); and

In response to the read signal (read message commend), transmit the first data packet from the ancillary memory to another location (message output register sends the message to the processor who issued the read commend), and replenish the ancillary memory by transferring a stored data packet of the message to the ancillary memory from the main memory (message is retrieved from the addressed mailbox entry and placed in message output register)(see, e.g., col. 6, lines 48-57).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 10, 17 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bolan al. (hereinafter Bolan)(U.S. Patent No. 5,210,828) as applied to claims 9, 16 and 21 above, and further in view of Ternes et al. (hereinafter Ternes)(U.S. Patent No.

4,935,894).

Regarding claims 10, 17 and 22, Bolan teaches all the limitations of claim except for teaching of using FIFO register as an ancillary memory.

Ternes teaches as follows:

Bus interface circuit (40 and 50 in figure 2) comprises a first-in-first-out (FIFO) register stack (55 and 60 in figure 2), interrupt logic, and transmitter/receiver logic. The pair of bus interface circuits provides dual simplex data and control transfer between the two buses (see, e.g., col. 2, lines 46-50 and figure 2).

It would have been obvious for one of ordinary skill in the art at the time of the invention to modify Bolan to include FIFO register as a buffer memory as taught by Ternes in order to process multiple packets in sequence between two processors.

6. Claims 12, 15, 19, 24, 27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bolan al. (hereinafter Bolan)(U.S. Patent No. 5,210,828).

Regarding claims 12, 19, 24, 27 and 28, Bolan teaches as follows:

The control unit is further configured to transmit the stored data packet from the ancillary memory (message output register sends the message to the processor who issued the read commend) and replenish the ancillary memory (message is retrieved from the addressed mailbox entry and placed in message output register, see, e.g., col. 6, lines 48-57); and

Four clock cycles to decode and execute a command (see, e.g., col. 5, lines 56-68).

Bolan does not teach the clock cycle related to transmitting and replenishing

functions.

It would have been obvious for one of ordinary skill in the art at the time of the invention to modify Bolan to include clock cycle in order to provide time sequence process during the transmitting and replenishing functions.

Regarding claim 15, Bolan teaches as follows:

Message field segment contains the beginning and ending of address of the task control block located in main storage, see, e.g., col. 5, lines 27-33).

It would have been obvious for one of ordinary skill in the art at the time of the invention to modify Bolan to include message segmentation in order to transfer large size of message beyond the capacity of bus between two processors into multiple of proper packets.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeong S. Park whose telephone number is 571-270-1597. The examiner can normally be reached on Monday through Thursday 7:30 - 5:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SUPERVISORY PATENT EXAMINER
NATHAN FLYNN

JP

July 24, 2007